METHOD OF DEPOSITING A CONDUCTIVE NIOBIUM MONOXIDE FILM FOR MOSFET GATES

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BACKGROUND OF THE INVENTION

The present invention relates generally to methods of forming niobium monoxide and, more particularly, to methods of depositing niobium monoxide suitable for use as MOSFET gates.

As the gate length of silicon CMOS devices are scaled below 100nm, new high-k materials are expected to replace silicon dioxide as the gate insulating material, and new gate materials, including metal gates, are expected to replace polycrystalline silicon. These new gate materials are expected to solve the polysilicon gate depletion problem. The new gate materials may also enable threshold voltage adjustment without the need to alter the channel doping.

The new gate materials should have an appropriate work function. For CMOS devices, the gate materials should have a work function of approximately 4.2eV for NMOS gates. The gate materials should have a work function of approximately 5.0eV for the PMOS gates. It is possible to use different gate materials for the two different kinds of gates, NMOS and PMOS, in the CMOS process.

The new gate materials should be stable. NMOS metals are often highly reactive and normally unstable in contact with the gate dielectric. PMOS metals are more stable but more difficult to process. Even if chemically stable materials are identified, they should also be mechanically stable as well. The new gate materials should not exhibit

poor adhesion. The new gate materials should not diffuse into the channel.

It would be desirable to have new gate materials that could be integrated into existing IC processes, such as having deposition and etching process that can be incorporated into existing processes.

The available choices for new gate materials include elemental metals, binary alloys, ternary alloys or even more complex materials. There are many materials that may qualify as PMOS gate candidates. However, qualified NMOS gate candidates, having a low work function, are very limited. One of the challenges for NMOS gate candidates is having a low enough work function, for example around 4.2eV along with good stability in contact with the gate dielectric.

Binary alloys of RuTa or MoN have been explored. By altering the composition of these binary metal alloys it is possible to control the work function of the resulting material. However, when the work function of these alloys is targeted to values suitable for NMOS gates, work function below 4.3eV, the thermal stability tends to deteriorate.

SUMMARY OF THE INVENTION

Accordingly, methods are provided to deposit conductive niobium monoxide films as MOSFET gates.

A metal target of Nb is provided in a sputtering chamber. A substrate comprising a gate dielectric material is introduced into the chamber. The sputtering power and oxygen partial pressure are selected to deposit a niobium monoxide film, while reducing, or eliminating, insulating phases of the metal oxides. The sputtering power and oxygen

partial pressure may also be selected to reduce, or eliminate, elemental metal from the deposited film.

In another embodiment, a composite target of NbO is provided in a sputtering chamber. A substrate comprising a gate dielectric material is introduced into the chamber. The sputtering power and oxygen partial pressure are selected to deposit a niobium monoxide film, while reducing, or eliminating, insulating phases of the metal oxides. Because of the use of a composite target, additional oxygen may not be needed at all, although in some cases some oxygen may be used. The sputtering power and oxygen partial pressure may also be selected to reduce, or eliminate, elemental metal from the deposited film.

BRIEF DESCRIPTION OF THE DRAWINGS

Fig. 1 shows XRD plots.

Fig. 2 shows XRD plots.

Fig. 3 shows XRD plots.

Fig. 4 shows a plot of work function versus anneal temperature.

Fig. 5 shows a cross-sectional view of a gate structure during CMOS processing.

Fig. 6 shows a cross-sectional view of a gate structure during CMOS processing.

Fig. 7 shows a cross-sectional view of a gate structure during CMOS processing.

Fig. 8 shows a cross-sectional view of a gate structure during replacement gate CMOS processing.

Fig. 9 shows a cross-sectional view of a gate structure during replacement gate CMOS processing.

Fig. 10 shows a cross-sectional view of a gate structure during replacement gate CMOS processing.

DETAILED DESCRIPTION OF THE INVENTION

Niobium monoxide (NbO) is characterized by a high conductivity, which is a property usually associated with metals. The reaction between Nb and O is exothermic, which makes it difficult to control the reaction and prevent Nb_2O_5 from being formed. Nb_2O_5 is an insulator, which would not be suitable for use as a gate material. Nb and O may also combine to from NbO_2, which is also not suitable for use as a gate material. For our purposes we will use NbO_x to refer generally to niobium oxides without regard to a specific phase. NbO will refer specifically to materials comprising niobium monoxide. The present method provides a means of depositing a predominantly NbO film, which means a NbO film that may contain some other phases of niobium oxide, or elemental niobium. The term NbO gate, NbO film, and NbO material refer herein to materials comprised of predominantly NbO with levels of impurities including NbO_2, or elemental niobium, which are at levels that will not prevent the NbO from acting as an NMOS gate.

For the following examples, an Edwards Auto 306 DC magnetron sputtering system was used with a 99.95% pure Nb target. Argon and oxygen gases were introduced. A total pressure of 6 mtorr was maintained during film deposition. The oxygen content of the NbOx film is controlled by adjusting the partial pressures of oxygen $[P_{O2}/(P_{O2}+P_{Ar})]$. The relative oxygen content of the deposited NbOx film is also changed by

varying the sputtering power. By adjusting these parameters it is possible to produce a predominantly NbO film. After sputtering the as deposited films were annealed at approximately 800 degrees Celsius for approximately 5 minutes in argon. Fig. 1 shows the x-ray diffraction (XRD) measurements associated with the following three examples.

Example 1:

A 300W sputtering power was used with an O_2 partial pressure of approximately 30%. The O_2 partial pressure was established using mass flow controllers to control the amount of both O_2 and argon entering the sputtering chamber. The resulting film is a mix of NbO and NbO_2, which corresponds to XRD plot 12 in Fig. 1. The NbO peaks 14 indicate the presence of NbO, while the NbO_2 peaks 16 indicate the presence of NbO_2. The results of this example may not contain a sufficient amount of NbO to act as a suitable gate material, but the example is presented to illustrate the effect of changing oxygen partial pressure.

Example 2:

A 300W sputtering power was used with an O_2 partial pressure of approximately 25%. The O_2 partial pressure was established using mass flow controllers to control the amount both O_2 and argon entering the sputtering chamber. The resulting film, which corresponds to XRD plot 22, is predominantly NbO, with detectable levels of NbO_2. An NbO_2 peak 26 is still discernable, but the NbO peaks 24 are even more apparent than in Example 1. Although, some NbO_2 is present this predominantly NbO film is suitable for use as an NbO gate.

Example 3:

The sputtering power was increased to 350W while the O_2 partial pressure was maintained at approximately 25%. The O_2 partial pressure was established using mass flow controllers to control the amount both O_2 and argon entering the sputtering chamber. The resulting film, which corresponds to XRD plot 32, is predominantly NbO, without any discernable NbO_2 peaks. The NbO peaks 34 are even more apparent than in Example 2.

Among the three examples just provided, Example 3 provides a NbO film with the least amount of discernable NbO_2. Example 2 may still be suitable for use as an NbO gate, provided the increased resistivity caused by the NbO_2 does not significantly degrade the overall performance as an NMOS gate.

Fig. 2 shows XRD measurements for the material produced by Example 3, before and after anneal at approximately 800 degrees Celsius for approximately 5 minutes in argon. Fig. 2 shows that the as-deposited NbO film, which corresponds to XRD plot 42, has a broad peak around NbO (111). XRD plot 44 corresponds to the NbO film after anneal and shows additional peaks indicative of single phase NbO. The anneal increased crystal size from 2nm before anneal to 40nm after anneal. The anneal also reduced the resistivity of approximately 830 $\mu\Omega$-cm before anneal to approximately 82 $\mu\Omega$-cm.

The density of the NbO film produced using the process of Example 3 was determined to be approximately 7.55g/cm^3, which compares favorably with the published density for bulk NbO of 7.265g/cm^3.

Example 4:

Another method of sputtering NbO_x also uses the Edwards Auto 306 DC magnetron sputtering system with a 99.95% pure Nb target. The sputtering power of 300W was selected. In this example, instead of introducing separate sources of argon and oxygen a 15% O_2/Ar gas is used. Using a combined gas makes the process less subject to the uncertainty of the mass flow controllers. To adjust the O_2 partial pressure the 15% O_2/Ar flow rate was increased. Adjusting the flow rate changed the partial pressure because the Edwards system used has a constant pump rate. When the flow rate is increased the NbO_x film becomes oxygen rich. Decreasing the flow rate causes the NbO_x film to become oxygen deficient. In an alternative embodiment, a system may be used which allows the partial pressure to be adjusted by adjusting the flow rate, the pump rate, or a combination of both. Fig. 3 shows the XRD results for three films produced at 15% O_2/Ar flow rates of between approximately 2.65 sccm and 2.85 sccm after annealing at approximately 800 degrees Celsius for approximately 5 minutes in argon. The XRD plot 52 shows the NbO peaks along with an Nb peak 56, which indicates the presence of elemental niobium. The XRD plot 62 shows the NbO peaks without any discernable peaks suggesting elemental niobium or NbO_2. The XRD plot 72 shows the NbO peaks along with a peak 74 indicating the presence of NbO_2.

Fig. 4 shows the work function of an example of an NbO gate as a function of anneal temperature. This indicates that it is possible to achieve a NbO gate with stable work functions approaching approximately 4.2eV.

The NbO films produced according to the above method have a work function of approximately 4.2 ± 0.1 eV. The work function is stable, following an initial low temperature anneal at 400 degrees Celsius for 30 minutes in argon, up to subsequent anneal temperatures as high as 1000 degrees Celsius for 1 minute in argon. The NbO materials also demonstrated stability in contact with the gate dielectric, both silicon dioxide and high-k materials. For example, NbO films on ALD HfO_2 were tested by annealing at temperatures up to 1000 degrees Celsius. Following an 800 degrees Celsius anneal the effective oxide thickness (EOT) changed from 33 angstroms to 30 angstroms, but this value was then stable after 1000 degrees Celsius anneal.

The sputtering examples provided above tend to be equipment dependent. Those of ordinary skill in the art will be able to produce NbO films, without undue experimentation based upon the above examples, using different equipment by adjusting the O_2 partial pressure and the sputtering power.

Although in the examples provided argon was combined with O_2 to control the partial pressure, other gases may be used including neon, helium, krypton, xenon or a combination.

NbO can be deposited to form a MOSFET gate. In one embodiment, the MOSFET gate is fabricated using a standard CMOS flow. As shown in Fig. 5, a substrate 110 is provided. A gate dielectric material 112 is deposited overlying the substrate. The gate dielectric material is silicon dioxide, which may be deposited by thermal oxidation or plasma oxidation of a silicon substrate, or a high-k dielectric material, such as HfO_2, ZrO_2, Ta_2O_5, or Al_2O_3. A layer of niobium monoxide 114 is then deposited overlying the gate dielectric material. As described above,

the layer of niobium monoxide can be deposited by sputtering, and adjusting the oxygen partial pressure, and the sputtering power to control the amount of oxygen incorporated into the film to produce a niobium monoxide film, without significant amounts of oxygen rich insulating phases of the NbO_x being incorporated in to the film. The niobium monoxide 114 is then annealed as described above. A layer of photoresist 116 is then deposited and patterned.

As shown in Fig. 6, source and drain regions 122 are implanted and activated. The activation anneal for the source and drain regions may serve to further anneal the niobium monoxide 114. In an embodiment of the present method no additional anneal is required. In another embodiment an additional anneal of the niobium monoxide 114 may be performed prior to the formation of the source and drain. Any anneal of the niobium monoxide material is preferably done in the absence of oxygen. The niobium monoxide material 114 is then etched to form a gate 124.

The photoresist is then removed, as shown in Fig. 7. Additional processing may then be performed to complete the device, including for example depositing insulating material and then forming contacts to the gate 124, and the source and drain regions 122.

In an embodiment of the present method, the ashing steps may expose the surface of the gate 124 to oxygen. This oxygen will tend to oxidize the gate forming a surface layer of insulating material. This surface layer of insulating material may not degrade the gate performance. A portion of the surface insulating material will be removed when the gate contact is formed, so that contact can be made to the gate.

If the oxidation caused by annealing in oxygen or ashing is determined to degrade the gate unacceptably, care can be taken to reduce, or eliminate, oxygen during the annealing or ashing processes to reduce, or eliminate, the oxidation of the gate. A capping layer (not shown) may be used to protect the gate from unwanted oxygen exposure. The capping layer may surround the gate, or if sidewalls are present the capping layer may just cover the exposed upper surface of the gate. In one embodiment, the capping layer is composed of a material, for example silicon nitride. During subsequent contact etching a portion of this capping layer will be removed to make electrical contact with the gate. In another embodiment, the capping layer is a conductive barrier metal, such as TiN, which may be deposited immediately after the niobium monoxide, to form a TiN/niobium monoxide gate stack. The capping layer may be deposited prior to depositing and patterning the photoresist.

Referring now to Figs. 8-10, NbO can be incorporated into replacement gate CMOS process flow. In one embodiment, a substitute gate (not shown) is formed and used align the source and drain implantation, and anneal processes. An insulating material 311 is then deposited over the substitute gate and planarized to expose the substitute gate. The substitutes gate is then removed leaving a trench 300, which exposes the channel region of the substrate, as shown in Fig. 8, or a previously formed gate dielectric.

A gate dielectric 330 can be deposited into the trench 300 as shown in Fig. 9. A layer of niobium monoxide 318 is then deposited over the gate dielectric. The layer of niobium monoxide 318 may be sputter deposited to a thickness of about 1.5 times the depth of the trench.

Alternatively, the gate dielectric layer may have been formed prior to the formation of the substitute gate. The removal of the substitute gate would then expose the gate dielectric layer, and a layer of niobium monoxide 318 could be deposited over the gate dielectric layer.

Fig. 10 shows an embodiment of a transistor structure using a replacement gate process flow, following planarization of the layer of niobium monoxide and the gate dielectric to form a dielectric layer 416, and a niobium monoxide gate 418. A CMP process may be used to accomplish the planarization. Additional processing may be used to complete the transistor structure and provide electrical contact to the gate 418 and the source and drain regions 422.

Several embodiments have been provided as examples. The scope of the present invention should not be limited to these examples, and shall be determined by the following claims.